Amendments to the Specification:

Please replace the paragraph, beginning at page 1, line 18, with the following rewritten paragraph:

Fig. 12 shows a <u>an example of a prior art</u> configuration example of such a voltage-controlled oscillator-in the past.

In Fig. 12, reference numerals 1a and 1b denote oscillation transistors, 2a and 2b denote inductors, and 3a and 3b denote variable capacitance elements. Reference numeral 4 denotes a power supply terminal, 5 denotes a frequency control terminal, and 6 denotes a current source. A bias circuit and so onother elements are omitted in Fig. 12.

Please delete the paragraph, beginning at page 2, line 1:

Hereafter, operation of the voltage controlled oscillator in the past will be described by referring to Fig. 12.

As an oscillation frequency of the voltage-controlled oscillator oscillates in the neighborhood of the resonance frequency of the resonant circuit, it is possible, by adjusting the control voltage, to control the oscillation frequency of the voltage-controlled oscillator to be a desired frequency. The oscillation transistors 1a and 1b are intended to generate negative resistance and cancel losses due to a parasitic resistance component of the resonant circuit so as to satisfy an oscillation requirement.

Please replace the paragraph, beginning at page 2, line 21, with the following rewritten paragraph:

Here, a A relationship between the control voltage and the oscillation frequency of the voltage-controlled oscillator is virtually determined by a characteristic of the variable capacitance element. It is desirable that and so the variable capacitance element to be used is desired to changes the capacitance slowly in a wide range of the control voltage. It is because, in the case of constituting a PLL (phase lock loop) by using the voltage-controlled oscillator, a transient response characteristic and a noise band characteristic of a PLL circuit depend on frequency sensitivity against with respect to the control voltage. Therefore, if the frequency sensitivity is different according to the frequency, the characteristic of the PLL circuit itself changes according to the frequency. In an area where the frequency sensitivity against with respect to the control voltage is high, there is a problem that a phase noise characteristic is degraded because the frequency changes due to slight noise caused on a frequency control terminal.

Please replace the paragraph, beginning at page 3, line 13, with the following rewritten paragraph:

In reality, however, it is difficult to utilize the variable capacitance element of high linearity because. The reason for this is that when implementing the voltage-controlled oscillator is formed on a semiconductor substrate, the costs are increased by introducing on a special process for the sake of needed to forming the variable capacitance element. Fig. 13 (a) shows the variable capacitance element utilizing a gate capacitance widely used in a CMOS process, and Fig. 13 (b) shows the variation of the gate capacitance in the case of applying the reference voltage to the gate of a MOS transistor and applying the control voltage to a drain-source side. Thus, in the case of the variable capacitance element utilizing the gate capacitance of the MOS transistor generally used, the capacitance value abruptly changes in the neighborhood of a threshold voltage (Vth in the drawing). -so that Thus, the oscillation frequency also abruptly changes in an area in the neighborhood of a threshold. Consequently, there arises a problem that the transient response characteristic and noise band characteristic of the PLL circuit using this VCO significantly change depending on the frequency.

Please delete the paragraph, beginning at page 4, line 8:

The circuit described below has already been proposed in order to solve such problems.

Please replace the paragraph, beginning at page 4, line 10, with the following rewritten paragraph:

Fig. 14 is the-a circuit showing a technique of improving the linearity of the variable capacitance element in the past (refer to Japanese Patent Laid-Open No. 2001-352218 for instance). In Fig. 14, the same portions as those previously described are given the same symbols and a description thereof will be omitted.

Please replace the paragraph, beginning at page 5, line 5, with the following rewritten paragraph:

In the above method, the level shift circuit 13 is constituted by using the transistors such as FET as shown in Fig. 22. It-This is because the level shift circuit 13 requires high input impedance in order to hold a DC voltage inputted from the frequency control terminal 5.

Please replace the paragraph, beginning at page 5, line 22, with the following rewritten paragraph:

As a countermeasure-against it, there is ahas been proposed a configuration wherein one voltage applied to each variable capacitance element is not the power supply voltage, and each variable capacitance element is interrupted from the power supply voltage with a blocking capacitor so as to supply the reference voltage different from the power supply voltage (refer to "Prospects of CMOS Technology for High-Speed Optical Communication Circuits" by Behzad Razavi, IEEE Journal of Solid-State Circuit, vol. 37, No. 9 September 2002, pp. 1135 – 1144 for instance).